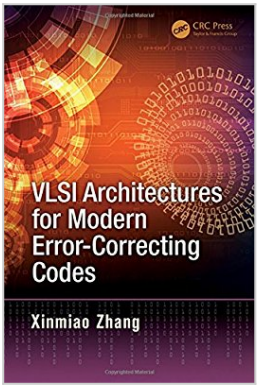

VLSI Architectures for Modern Error-Correcting Codes

By Xinmiao Zhang

VLSI Architectures for Modern Error-Correcting Codes By Xinmiao Zhang

Error-correcting codes are ubiquitous. They are adopted in almost every modern digital communication and storage system, such as wireless communications, optical communications, Flash memories, computer hard drives, sensor networks, and deep-space probing. New-generation and emerging applications demand codes with better error-correcting capability. On the other hand, the design and implementation of those high-gain error-correcting codes pose many challenges. They usually involve complex mathematical computations, and mapping them directly to hardware often leads to very high complexity.

VLSI Architectures for Modern Error-Correcting Codes serves as a bridge connecting advancements in coding theory to practical hardware implementations. Instead of focusing on circuit-level design techniques, the book highlights integrated algorithmic and architectural transformations that lead to great improvements on throughput, silicon area requirement, and/or power consumption in the hardware implementation.

The goal of this book is to provide a comprehensive and systematic review of available techniques and architectures, so that they can be easily followed by system and hardware designers to develop en/decoder implementations that meet error-correcting performance and cost requirements. This book can be also used as a reference for graduate-level courses on VLSI design and error-correcting coding. Particular emphases are placed on hard- and soft-decision Reed-Solomon (RS) and Bose-Chaudhuri-Hocquenghem (BCH) codes, and binary and non-binary low-density parity-check (LDPC) codes. These codes are among the best candidates for modern and emerging applications due to their good error-correcting performance and lower implementation complexity compared to other codes. To help explain the computations and en/decoder architectures, many examples and case studies are included.

More importantly, discussions are provided on the advantages and drawbacks of different implementation approaches and architectures.

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Editorial Review

Review

"Error-correction coding has become an ineluctable feature for the development of modern telecommunication and storage systems. The VLSI implementation of powerful error-correcting codes and decoders with a minimum hardware resource is especially of great importance for the integration of the codes in high-speed, low consumption circuits. Such implementation requires a deep understanding of both mathematical theory of the codes and VLSI architecture design of their decoders, a dual expertise that Dr. Xinmiao Zhang was able to transcribe with high rigor and clarity in this book. From cyclic codes to the more recent binary and non-binary LDPC codes, this book equips any engineer or researcher with the necessary knowledge to implement state-of-the-art solutions."
?Prof. David Declercq, Director General of Research at the ENSEA, Cergy-Pontoise, France

"This book is unique in its synthesis of the advanced concepts in abstract algebra, decoding algorithms and architecture used masterfully to introduce VLSI implementations of highly sophisticated decoders of modern error correction codes."
?Bane Vasic, University of Arizona

About the Author

Xinmiao Zhang received her Ph.D in electrical engineering from the University of Minnesota, Twin Cities, USA. Dr. Zhang is currently a principal research engineer at SanDisk, Milpitas, California, USA. Previously, she was a Timothy E. and Allison L. Schroeder assistant professor, and then a tenured associate professor, in the Department of Electrical Engineering and Computer Science at Case Western Reserve University, Cleveland, Ohio, USA. She has also been a visiting professor at Qualcomm and spent her sabbatical leave at the University of Washington, Seattle, USA. Her research focuses on VLSI architecture design for communications, digital signal processing, and cryptography. She is a recipient of the National Science Foundation Faculty Early Career Development (CAREER) Award.

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