



Physical Layer Multi-Core Prototyping: A Dataflow-Based Approach for LTE eNodeB: 171 (Lecture Notes in Electrical Engineering)

By Maxime Pelcat, Slaheddine Aridhi, Jonathan Piat, Jean-François Nezan

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Base stations developed according to the 3GPP Long Term Evolution (LTE) standard require unprecedented processing power. 3GPP LTE enables data rates beyond hundreds of Mbits/s by using advanced technologies, necessitating a highly complex LTE physical layer. The operating power of base stations is a significant cost for operators, and is currently optimized using state-of-the-art hardware solutions, such as heterogeneous distributed systems. The traditional system design method of porting algorithms to heterogeneous distributed systems based on test-and-refine methods is a manual, thus time-expensive, task.

Physical Layer Multi-Core Prototyping: A Dataflow-Based Approach provides a clear introduction to the 3GPP LTE physical layer and to dataflow-based prototyping and programming. The difficulties in the process of 3GPP LTE physical layer porting are outlined, with particular focus on automatic partitioning and scheduling, load balancing and computation latency reduction, specifically in systems based on heterogeneous multi-core Digital Signal Processors. Multi-core prototyping methods based on algorithm dataflow modeling and architecture system-level modeling are assessed with the goal of automating and optimizing algorithm porting.

With its analysis of physical layer processing and proposals of parallel programming methods, which include automatic partitioning and scheduling, *Physical Layer Multi-Core Prototyping: A Dataflow-Based Approach* is a key resource for researchers and students. This study of LTE algorithms which require dynamic or static assignment and dynamic or static scheduling, allows readers to reassess and expand their knowledge of this vital component of LTE base station design.

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- Sales Rank: #3802055 in eBooks
- Published on: 2012-08-11
- Released on: 2012-08-11
- Format: Kindle eBook

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Editorial Review

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Maxime Pelcat is an associate professor at the Department of Electrical and Computer Engineering at the National Institute of Applied Sciences (INSA) in Rennes. He holds a joint appointment in the Institute of Electronics and Telecommunications of Rennes (IETR), a CNRS research unit. Maxime Pelcat obtained his Ph.D. in signal processing from INSA in 2010. The Ph.D. thesis resulted from a collaboration of INSA Rennes and Texas Instruments, Nice, and followed a contract as research engineer. Previously, after one year in the Audio and Multimedia department at Fraunhofer-Institute IIS in Erlangen, Germany, he worked as a contractor at France Telecom Research and Development until 2006. His main research interests include dataflow models, multimedia and telecommunication processing, and programming of distributed embedded systems.

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applications for communications infrastructure. In his role as senior wireless systems engineer at Texas Instruments France (TIF), Dr. Aridhi is driving solution analyses for LTE and other emerging applications (e.g. small cells, backhaul,...) in addition to actively participating in the architecture definition of next generation devices. His efforts have enabled TI to take leadership positions in these evolving standard/proprietary applications. In his 17 years in the industry, Dr. Aridhi has gained extensive experience in wireless/digital communications research and development for digital communications, IP data networking, and wireless systems applications. Dr. Aridhi is also co-supervising a Ph.D. thesis on rapid prototyping and code generation for complex applications in collaboration with the INSA Rennes, France. Dr. Aridhi obtained his Ph.D. in wireless telecommunications from the INRS (Institut National de Recherche Scientifique) in Montreal, Canada. He also holds M.S. and B.S. degrees in Digital Communications and Electrical Engineering respectively from the University Laval in Quebec City, Canada.

Jonathan Piat is an associate professor at the department of Electrical and Computer Engineering at Paul Sabatier University of Toulouse (France). He holds a joint appointment in the Laboratory for Analysis and Architecture of Systems, a CNRS research unit. Dr Piat obtained his Phd thesis in electronic and signal processing from the INSA of Rennes in 2010. His work dealt with loop partitioning for dataflow models to target multi-core architectures with signal processing applications. He is now working on the integration of robotics algorithms on FPGA-based dedicated hardware. His main research interests include dataflow-models, hardware/software co-design, embedded vision processing and robotics.

Jean-Francois Nezan is a Professor at the Department of Electrical and Computer Engineering at the National Institute of Applied Sciences (INSA), Rennes Scientific and Technical University. Pr. Jean-Francois NEZAN holds a joint appointment in the Institute of Electronics and Telecommunications of Rennes (IETR). He is coauthor or coeditor of more than 40 technical articles and 2 patents. He supervised 6 defended PhDs and currently supervises 3 PhDs. Jean-François NEZAN is involved in the french research society “GDR ISIS” in the C theme entitled “adequation algorithm architecture”. He participated to the setting-up and the management of 4 founded national projects, 1 European project and 8 research agreements with industrial partners. He also participates to the setting-up of the Modae Technology Company. His research topic is the rapid prototyping of standard video compression on embedded architectures. Since 2007, he is involved in the MPEG standardization activities. His research interests include signal processing systems (video and telecommunication algorithms), embedded software, and hardware/software co-design.

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