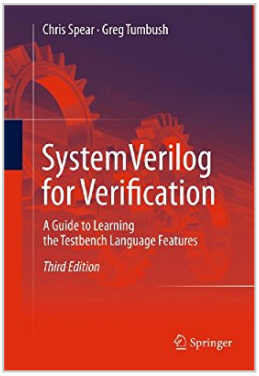

SystemVerilog for Verification: A Guide to Learning the Testbench Language Features

By Chris Spear, Greg Tumbush

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Based on the highly successful second edition, this extended edition of *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features* teaches all verification features of the SystemVerilog language, providing hundreds of examples to clearly explain the concepts and basic fundamentals. It contains materials for both the full-time verification engineer and the student learning this valuable skill.

In the third edition, authors Chris Spear and Greg Tumbush start with how to verify a design, and then use that context to demonstrate the language features, including the advantages and disadvantages of different styles, allowing readers to choose between alternatives. This textbook contains end-of-chapter exercises designed to enhance students' understanding of the material. Other features of this revision include:

- New sections on static variables, print specifiers, and DPI from the 2009 IEEE language standard
- Descriptions of UVM features such as factories, the test registry, and the configuration database
- Expanded code samples and explanations
- Numerous samples that have been tested on the major SystemVerilog simulators

SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Third Edition is suitable for use in a one-semester SystemVerilog course on SystemVerilog at the undergraduate or graduate level. Many of the improvements to this new edition were compiled through feedback provided from hundreds of readers.

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Editorial Review

From the Back Cover

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About the Author

Chris Spear has been working in the ASIC design and verification field for 30 years. He started his career with Digital Equipment Corporation (DEC) as a / CAD Engineer on DECsim, connecting the first Zycad box ever sold, and then a hardware Verification engineer for the VAX 8600, and a hardware behavioral simulation accelerator. He then moved on to Cadence where he was an Application Engineer for Verilog-XL, followed by a stint at Viewlogic. Chris is currently employed at Synopsys Inc. as a Verification Consultant, a title he created a dozen years ago. He has authored the first and second editions of *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features*. Chris earned a BSEE from Cornell University in 1981. In his spare time, Chris enjoys road biking in the mountains and traveling with his wife.

Greg Tumbush has been designing and verifying ASICs and FPGAs for 13 years. After working as a researcher in the Air Force Research Labs (AFRL) he moved to beautiful Colorado to work with Astek Corp as a Lead ASIC Design Engineer. He then began a 6 year career with Starkey Labs, AMI Semiconductor, and ON Semiconductor where he was an early adopter of SystemC and SystemVerilog. In 2008, Greg left ON Semiconductor to form Tumbush Enterprises, LLC where he has been consulting clients in the areas of design, verification, and backend to ensure first pass success. He is also a part time Instructor at the University of Colorado, Colorado Springs where he teaches senior and graduate level digital design and verification courses. He has numerous publications which can be viewed at www.tumbush.com. Greg earned a Ph.D. from the University of Cincinnati in 1998.

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